Intel Increases Transistor Speed by Building Upward

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HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

The transistors on computer chips — whether for PCs or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel’s co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

These early transistors were built on a flat surface. But like a real estate developer building skyscrapers to get more rentable space from a plot of land, Intel is now building up. When the space between the billions of tiny electronic switches on the flat surface of a computer chip is measured in the width of just dozens of atoms, designers needed the third dimension to find more room.

The company has already begun making its microprocessors using a new 3-D transistor design, called a Finfet (for fin field-effect transistor), which is based around a remarkably small pillar, or fin, of silicon that rises above the surface of the chip. Intel, based in Santa Clara, Calif., plans to enter general production based on the new technology some time later this year.
pany has already begun making processors using a new 3-D transistor (or fin field-effect transistor), which fits a relatively small pillar, or fin, of silicon in the surface of the chip. Intel, based in Santa Clara, entered general production based on...
What is a transistor?

control → input → output
Switching

1

\[
\text{on, current flows}
\]

0

\[
\text{off, no current flows}
\]
Amplification

gain
Transistor Operation

2-terminal device with nonlinear current-voltage curve.

\[ E = i_D R + v_D \]

steady-state operating conditions
Transistor Operation

3-terminal device with nonlinear current-voltage curves controlled by $v_G$.

\[ E = i_D R + v_D \]  Load line

small changes in $v_G$ $\rightarrow$ large changes in $v_D$ = amplification
what else do you need for faithful amplification? By changing $v_G$, we can change $i_D$ from 0 to $E/R$ = switching.
Junction Field-effect transistor

depletion regions exist in the lightly doped n region
This changes the width of the non-depleted n region (where carriers exist).

That in turn changes resistance of the n-channel & hence, changes current.

Thus, the gate voltage controls current flow from drain to source.
\[ V_{GG} = V_{GS} \]
The lightly-doped n-channel is a distributed resistor.

due to current flow, there is a voltage drop from drain to source.
Pinch-off & Saturation

At low current, voltage drop from drain to source is small. Depletion region is the same across the channel.

As current increases, the gate-channel junction is more reverse-biased near the drain than the source. This starts to limit current flow.

Further increase in current pinches off the channel as the two depletion regions meet. Current doesn't really increase much further as voltage is increased = saturation.

Which way is the electric field pointing in the channel?

Note: gate & source are connected.

$V_G = 0$

$V_{GD} = -V_D$

Pinched-off channel
Gate Control

Previously, the gate voltage was 0. What happens when we apply a reverse-biased gate voltage?

The depletion region becomes wider & pinch-off occurs at lower drain current. Negative gate voltage changes the I-V curve.

Beyond pinch-off, the gate voltage controls the drain current (not the drain voltage). If a small-ac signal is put at the gate, the drain current amplifies it!
How to calculate the pinch-off voltage?

Symmetric channel is assumed.

The depletion-region width here

\[ W(x = L) = \left[ \frac{2\epsilon (-V_{GD})}{qN_d} \right]^{1/2} \] (V_{GD} negative)

Here, we assume contact potential is small.

Pinch-off occurs when

\[ h(x = L) = a - W(x = L) = 0 \]

Pinch-off voltage is then

\[ V_p = \frac{qa^2N_d}{2\epsilon} \]

where,

\[ V_p = -V_{GD}(\text{pinch-off}) = -V_G + V_D \]

What happens if V_G becomes positive, i.e., the gate-drain junction is forward biased?
Current-voltage characteristics of the JFET

The voltage drop in this infinitesimal length of the channel is related to current by

\[ I_D = \frac{Z2h(x)}{\rho} \frac{dV_x}{dx} \]

Depth of channel

\[ h(x) = a - W(x) = a - \left[ \frac{2\epsilon(-V_G)}{qN_d} \right]^{1/2} \]

Gradual-channel approximation:

\[ V_p = qa^2N_d/2\epsilon \]

 Resistivity of neutral n-region

Solving this, we get:

\[ I_D = G_0 V_P \left[ \frac{V_D}{V_P} + \frac{2}{3} \left( -\frac{V_G}{V_P} \right)^{3/2} \right] - \frac{2}{3} \left( \frac{V_D - V_G}{V_P} \right)^{3/2} \]

\[ G_0 = 2aZ/\rho L \]  conductance of the channel at 0 gate voltage & low drain current.

Below pinch-off

Putting these 2 equations together,

\[ \frac{2Za}{\rho} \left[ 1 - \left( \frac{V_x - V_G}{V_P} \right)^{1/2} \right] dV_x = I_D dx \]
At pinch-off, we have \( V_D - V_G = V_p \)

If we assume that beyond pinch-off, the current doesn't change, then the saturation current is

\[
I_{D\text{ (sat.)}} = G_0 V_p \left[ \frac{V_D}{V_p} + \frac{2}{3} \left( -\frac{V_G}{V_p} \right)^{3/2} - \frac{2}{3} \right]
\]

\[
= G_0 V_p \left[ \frac{V_G}{V_p} + \frac{2}{3} \left( \frac{V_G}{V_p} \right)^{3/2} + \frac{1}{3} \right]
\]

This gives rise to a family of curves.

As \( V_G \) becomes more negative, the saturation current decreases.

A small-signal voltage at the gate can be amplified if operating in the saturation regime!
For amplification, the device must operate under saturation. The input is gate voltage & the output is the drain-to-source current (saturated).

The amplification factor is defined by the mutual transconductance.

\[ g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} = G_0 \left[ 1 - \left( \frac{V_G}{V_P} \right)^{1/2} \right] \]

The figure of merit of a FET device is the mutual transconductance per unit depth.

Experimentally, the saturation drain current is related to the gate voltage as

\[ I_D(sat.) = I_{DSS} \left( 1 + \frac{V_G}{V_P} \right)^2, \quad (V_G \text{ negative}) \]

Two assumptions break down when the channel length is small (scaling for Moore's law)

A small drain-source voltage \( \rightarrow \) very high electric field in channel.

This can cause electron mobility to saturate & thereby increases resistivity with increasing voltage.

As drain voltage increases above pinch-off, the channel length decreases \( \rightarrow \) \( I_D(sat) \) can increase (not remain constant). Why?
Two assumptions break down when the channel length is small (scaling for Moore's law).

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**Metal-semiconductor FET (MESFET)**

Same as JFET, but using a reverse-biased Schottky barrier as the junction

- **S** (Source)
- **G** (Gate)
- **D** (Drain)

Metal-semiconductor (Schottky) barrier (Al)

Ohmic contacts (Au-Ge)

Semi-insulating GaAs

n GaAs

**Explain how this device works to your neighbor.**

- High-frequency operation --> microwave circuits.
- Small device size --> high-density integration.
- Used for GaAs integrated circuits.

Device characteristics are same as JFETs.
Short-channel Effects

If the channel length is 43nm and drain-source voltage is 1V, what is the electric field?

~230kV/cm!

Under this situation, mobility saturates.

Under mobility saturation, current is

$$I_D = qn_0 v_s A = qN_d v_s Z h$$

current saturates without pinch-off.

transconductance is independent of gate voltage.
Metal-Oxide Semiconductor FET (MOSFET)
The diagram illustrates a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) with the following components:

- **Source (S)**: The negative terminal.
- **Gate (G)**: The controlling terminal, connected to a positive voltage.
- **Drain (D)**: The positive terminal.
- **Oxide Layer**: A layer insulating the gate from the source and drain.
- **p-type substrate**: The semiconductor material.
- **n+ regions**: These are regions doped with more n-type material, typically used for the connections to the source and drain.
- **Body (B)**: Another terminal connected to the drain.

The gate voltage controls the flow of charge carriers between the source and drain, allowing the MOSFET to act as a switch.
MOSFET Qualitative Analysis

Three regimes of operation:

- **Cut-off regime**:
  - MOSFET: $V_{GS} < V_T$, $V_{DD} < V_T$ with $V_{DS} > 0$.
  - Water analogy: gate closed; no water can flow regardless of relative height of source and drain reservoirs.
  
- **Saturation regime**:
  - MOSFET: $V_{GS} > V_T$, $V_{DS} < V_T$ ($V_{DS} > 0$).
  - Water analogy: gate open; water flows from source to drain, but the height difference between the reservoirs affects the flow.

- **Linear regime**:
  - MOSFET: $V_{GS} > V_T$, $V_{DS} > V_T$ with $V_{DS} > 0$.
  - Water analogy: gate open but small difference in height between source and drain; water flows.

Electrons drift from source to drain → electrical current:

- $V_{GS} \rightarrow Q \rightarrow I_D$
- $V_{GS} \rightarrow I_D \rightarrow I_D$

$I_D$ is independent of $V_{GS}$: $I_D = I_{DS}$.

Pinch-off occurs when $V_D = V_T$.
Water analogy of MOSFET:

- **Source**: water reservoir
- **Drain**: water reservoir
- **Gate**: gate between source and drain reservoirs

Want to understand MOSFET operation as a function of:

- gate-to-source voltage (gate height over source water level)
- drain-to-source voltage (water level difference between reservoirs)

Initially consider source tied up to body (substrate or back).
Three regimes of operation:

- **Cut-off regime:**
  - MOSFET: $V_{GS} < V_T$, $V_{GD} < V_T$ with $V_{DS} > 0$.
  - Water analogy: gate closed; no water can flow regardless of relative height of source and drain reservoirs.

$$I_D = 0$$
Linear or Triode regime:

- MOSFET: $V_{GS} > V_T$, $V_{GD} > V_T$, with $V_{DS} > 0$.
- Water analogy: gate open but small difference in height between source and drain; water flows.

Electrons drift from source to drain $\Rightarrow$ electrical current!

- $V_{GS} \uparrow \rightarrow |Q_n| \uparrow \rightarrow I_D \uparrow$
- $V_{DS} \uparrow \rightarrow E_y \uparrow \rightarrow I_D \uparrow$
Saturation regime:

- MOSFET: $V_{GS} > V_T$, $V_{GD} < V_T$ ($V_{DS} > 0$).
- Water analogy: gate open; water flows from source to drain, but free-drop on drain side $\Rightarrow$ total flow independent of relative reservoir height!

$I_D$ independent of $V_{DS}$: $I_D = I_{Dsat}$
linear region for $V_G > V_T$ and $V_D < (V_G - V_T)$:

Pinch-off starts. Current saturates.

$V_G > V_T$ and $V_D = (V_G - V_T)$

Strong saturation.

$V_G > V_T$ and $V_D > (V_G - V_T).$